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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/493,033	01/28/2000	Nobuyuki Yoshii	32178.157339	1679

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VENABLE, BAETJER, HOWARD AND CIVILETTI, LLP
P.O. BOX 34385
WASHINGTON, DC 20043-9998

EXAMINER
SORRELL, ERON J

ART UNIT	PAPER NUMBER
2182	8

DATE MAILED: 04/09/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/493,033	Applicant(s) YOSHII, NOBUYUKI	
	Examiner Eron J Sorrell	Art Unit 2182	

-- The MAILING DATE of this communication appears n the cover sheet with the correspondenc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-8 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-8 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 January 2000 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing R view (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 4 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed 1/28/00 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-3 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Khera (U.S. Patent No. 4,723,204).

5. Referring to claim 1, Khera teaches A packet communication apparatus for processing consecutive fixed-length packets, the apparatus comprising:

a storage circuit (see lines 49-59 of column 1);

a first processing circuit which access the storage circuit for executing first processing with respect to data obtained from each of the packets (see lines 49-59 of column 1);

a second processing circuit which accesses the storage circuit for executing second processing with respect to data stored in the storage circuit; (see lines 49-59 of column 1); and

an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of the packets, the allocation circuit allocating a first time of the packet processing time to the first processing circuit for accessing the storage circuit and a second time of the packet processing time to the second processing circuit for accessing the storage circuit for accessing the storage circuit, the first time and the second time prevented from overlapping

with each other (see lines 60-67 of column 1 and lines 1-10 of column 2).

6. Referring to claim 2, Khera teaches the storage circuit is a DRAM and he second processing circuit refreshes the DRAM during a second time (see lines 60-67 of column 1).

7. Referring to claim 3, Khera teaches a producing circuit which receives a first packet synchronizing signal having first signal components each indicative of a boundary time point between the adjacent packets and produces a second packet synchronizing signal based on the first packet synchronizing signal, wherein the producing circuit, in response to one of the first signal components, produces in sequence second signal components of the second packet synchronizing at a given cycle corresponding to the packet processing time, the given cycle being free of an influence of the first signal components subsequent to the one of the first signal components, and wherein the allocation circuit executes the access time allocation based on the second packet synchronization signal (see item labeled 150 which is further illustrated in figure 2 and lines 20-67 of column 2 and lines 1-13 of column 3).

8. Referring to claim 8, Khera teaches a packet communication apparatus for processing consecutive fixed-length packets, the apparatus comprising:

a DRAM (see abstract);

a processing circuit which accesses said DRAM for processing data obtained from each of the packets (see item labeled 110 in figure 1);

a refresh circuit for refreshing the DRAM (see item labeled 150 in figure 2);

an allocation circuit for executing access time allocation with respect to a packet processing time allowed for processing each of the packets, the allocation circuit allocating a first time of the packet processing time to the processing circuit for accessing the DRAM and a second time of the packet processing time to the refresh circuit for refreshing the DRAM, the first time and second time prevented from overlapping with each other.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at

> the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Khera.

11. Referring to claims 4, 5, and 6, along with all of the limitations addressed in claim 3, Khera also discloses the producing circuit comprises a counter which produces in sequence the second signal components, at a given cycle in response to the one of the first signal components at the given cycle in response to the one of the first signal components (see item labeled 7 in figure 2).

Khera fails to disclose a control circuit, which inhibits any of the first signal components being asynchronous with the given cycle from being inputted into the counter.

It would have been obvious to one of ordinary skill in the art at the time of the applicant's invention to modify the apparatus of Khera such that it inhibits any of the first signal components being asynchronous with the given cycle from being inputted into the counter. Asynchronous data is often synchronized before entering any sequential device in order to prevent metastabitilty or undesirable conditions that occur because asynchronous events occur causing the system clock to

skew. It is for that reason that one of ordinary skill in the art at the time of the applicant's invention would have been motivated to make such modification.

12. Referring to claim 7, Khera, as applied to claim 4-6 above, discloses the producing circuit comprises a second counter (see item labeled 8 in figure 2) and in response to an input of each of the first signal components, outputs a corresponding signal component to the control circuit at a given cycle corresponding to the packet processing time.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following references are cited because they further show the state if the art as it pertains to process time allocation for storage devices:

U.S. Patent No. 4,611,275 to Garneir

U.S. Patent No. 5,752,266 to Miyawaki et al.

U.S. Patent No. 5,301,332 to Dukes

U.S. Patent No. 5,261,109 to Cadambi et al.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eron J

Sorrell whose telephone number is 703 305-7800. The examiner can normally be reached on Monday-Friday 9:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffery A Gaffin can be reached on 703 308-3301. The fax phone numbers for the organization where this application or proceeding is assigned are 703 746-7239 for regular communications and 703 746-7238 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703 305-3900.

EJS
April 5, 2003

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100